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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,561	01/22/2004	Christopher A. Menkus	08211/0200350-US0/P05787	4900

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EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/19/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/763,561	MENKUS ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 – 3, 6 – 12, and 14 – 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,6-10,15 and 28* is/are allowed.

6)☒ Claim(s) *11, 12, and 17 – 26* is/are rejected.

7)☒ Claim(s) *14,16 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to amendment filed on 11/30/06. Claims 1 – 3, 6 – 12, and 14 – 28 are pending on this application.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 11, 15, 20, 21, 23 – 26 and 28 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 11, 12, and 17 – 26 are rejected under 35 U.S.C. 102(a) as being anticipated by Murphy U.S. Patent No. 6,157,257

Regarding claim 11, Fig. 1 of Murphy discloses a circuit, comprising: an amplifier array circuit (Q1 ...Q18) with a plurality of buses (101,102) for a folding analog-to-digital converter circuit (Col. 1 lines 3 - 6), wherein the amplifier array circuit (Q1 ...Q18) is a folding amplifier array circuit for a fine channel stage of the folding analog-to-digital converter (col. 2 lines 1 - 5) the amplifier array circuit comprising: a plurality of transconductance circuits circuit (Q1 ...Q18); a plurality of load circuits (RL1, RL2),

wherein each of the plurality of load circuits (RL1, RL2), is separately coupled to one of the plurality of buses (101, 102), wherein a first bus (101) of the plurality of buses is coupled to a portion (Q1, Q2, Q3) of the plurality of transconductance circuits (Q1 ...Q18); and a first current source circuit (ISUB1), wherein the first current source circuit is coupled to an output of a first of the portion (Q1, Q2, Q3) of the plurality of transconductance circuits, and wherein the first current source circuit (ISUB1) is arranged to provide a first local current (ISUB1) at the output of the first transconductance circuit (Q1) such that a maximum magnitude of current density is decreased (Col. 4 lines 51 - 53) on at least the first bus (101) of the plurality of buses; and another current source circuit (ISUB2) that is coupled to an output of another transconductance circuit (Q10) in the portion of transconductance circuits (Q1...Q18).

Regarding claim 12, wherein one of the portions of the transconductance circuits is not saturated (Q1, Q10), and wherein every other transconductance circuit in the portion is saturated (Q9, Q18).

Regarding claim 17, wherein the first transconductance circuit (Q1) is configured to provide the first transconductance current (output current of Q1) in response to a differential voltage (V1P); the first transconductance current is differentia (differential amplifier (Q1, A10); and wherein the first local current (ISUB1) is differential.

Regarding claim 18, wherein the first transconductance circuit (Q1, Q10) includes: a first differential pair (Q1, Q10); and a first tail current source (IT1) that is configured to provide a first tail current (IT1), and wherein the first local current (ISUB1) corresponds to a portion of the first tail current (IT1).

Regarding claim 19, wherein the portion of the first tail current is approximately half of the first tail current (since tail current IT1 is the sum of all currents at the nodes 101, 102 of Q1, Q10; thereby the portion current Q1 or Q10 must be approximate ½ of the tail current IT1).

Regarding claim 20, Fig. 1 of Murphy discloses a circuit for decreasing current density (Col. 4 lines 51 - 53) on a bus (101, 102) comprising: means (Q1...Q18) for folding analog-to-digital conversion (col. 1 lines 4 – 6), including: means (Q1) for amplifying a first input signal (V1P) to provide a first current (output current of Q1) to the bus 9101); means for providing a first local current (ISUB1); and means for canceling (Col. 4 lines 51 – 53) out at least a portion of the first current (output current of Q1) with the first local current (ISUB1) such that a maximum magnitude of a total current (current on bus 101) on the bus is reduced (Col. 4 lines 51 – 53).

Regarding claim 21, the claim incorporated the same subject matter as of claim 11, and rejected along the same rationale.

Regarding claim 22, wherein the bus is composed of metal having substantially no resistance (bus lines 101, 102).

Regarding claim 23, Fig. 1 of Murphy discloses a circuit for reducing the current density (Col. 4 lines 51 - 53) on a bus (101, 102) coupled to a plurality of circuits (Q1... Q18), the circuit comprising: a first amplifier circuit (Q1) of the plurality of circuits, wherein the first amplifier circuit (Q1) is configured to provide a first output current (current output of Q1) for the bus (101); a first current source circuit (ISUB1) that is arranged to provide a first local current (ISUB1) at an output of the first amplifier circuit

(Q1) such that at least a portion of the first output current is prevented from being carried on the bus (Col. 4 lines 51 - 53); and a load circuit (RL1) that is coupled to the bus (101), wherein the load circuit (RL1) is configured to provide an output voltage (X) such that the output voltage is substantially equal to the multiplicative product (Q1, Q2, Q3,.., Q9) of the bus current (101), and an impedance (RL1) of the load circuit.

Regarding claim 24, Fig. 1 of Murphy discloses a circuit for reducing the current density (Col. 4 lines 51 - 53) on a bus (101) coupled to a plurality of circuits (Q1, Q2, Q3), the circuit comprising: a first amplifier circuit (Q1) of the plurality of circuits, wherein the first amplifier circuit (Q1) is configured to provide a first output current (output current Q1) for the bus (101); a first current source circuit that (ISUB1) is arranged to provide a first local current (ISUB1) at an output of the circuit (X) such that at least a portion of the first output current (output current of Q1) is prevented from being bus Col. 4 lines 51 - 53); and load circuit (RL1) that is coupled to the bus (101), wherein the load circuit (RL1)does not include averaging impedances (RL1 does not discloses average impedance).

Regarding claim 25, Fig. 1 Murphy discloses a circuit for reducing the current density Col. 4 lines 51 - 53) on a bus (101) coupled to a plurality of circuits (Q1...Q9), the circuit comprising: a first amplifier circuit (Q1) of the plurality of circuits, wherein the first amplifier circuit (Q1) is configured to provide a first output current (output current of Q1) for the bus (101); a first current source circuit (ISUB1) that is arranged to provide a first local current (ISUB1) at an output of the first amplifier circuit (Q1) such that at least a portion of the first output current (output current of 24A) is prevented Col. 4 lines 51 -

53) from being carried on the bus (101); and a load circuit (RL1) that is coupled to the bus (101), wherein the load circuit (RL1) is coupled to a supply voltage (Voltage supply N01).

Regarding claim 26, Fig. 1 of Murphy discloses a circuit for reducing the current density (Col. 4 lines 51 - 53) on a bus (101) coupled to a plurality of circuits (Q1, Q2...), the circuit comprising: a first amplifier circuit (Q1) of the plurality of circuits (Q1, Q2, Q3..,Q9), wherein the first amplifier circuit (Q1) has at least an output (output current of Q1) that is connected to the bus (101), and wherein the first amplifier circuit (Q1) is configured to provide a first output current (output current of Q1) at the output of the first amplifier circuit; a first current source circuit (ISUB1) having at least an output (common output node X), wherein the output of the first current source circuit (ISUB1) is connected to the bus (101), and wherein the first current source circuit (ISUB1) is arranged to provide a first local current (ISUB1) at an output of the first current source circuit (ISUB1) such that at least a portion of the first output current (output current of Q1) is prevented Col. 4 lines 51 - 53) from being carried on the bus (101); and a second amplifier circuit (Q2) of the plurality of circuits, wherein the second amplifier circuit has at least an output (output of Q2) that is connected to the bus (101) , and wherein the second amplifier circuit (Q1) is configured to provide a second output current (output current of Q2) at the output of the second amplifier circuit (Q2).

Allowable Subject Matter

5. Claims 14 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not teach comprising: a plurality of current source circuits that includes the first current source circuit wherein each of the plurality of transconductance circuits has an output coupled to a separate one of the plurality of current source circuits.

6. Claim 27 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not teach a second current source circuit having at least an output wherein the output of the second current source circuit is connected to the bus, and wherein the second current source circuit is arranged to provide a second local current at an output of the second current source circuit such that at least a portion of the second output current is prevented from being carried on the bus.

7. Claims 1 – 3, 6 – 10, 15, and 28 are allowed.

With respect to claim 1, in addition to other elements in the claim, prior art considered individual or combination does not teach or suggest a circuit for reducing the current density on a bus comprising: a second amplifier circuit of the plurality of circuits, wherein the second amplifier circuit is configured to provide a second output current for the bus; and a second current source circuit that is configured to provide a second local

current at an output of the second amplifier circuit such that at least a portion of the second output current is prevented from being carried on the bus.

With respect to claim 15, in addition to other elements in the claim, prior art considered individual or combination does not teach or suggest amplifier circuit comprising: a plurality of current source circuits that includes the first current source circuit, wherein each of the plurality of transconductance circuits has an output coupled to a separate one of the plurality of current source circuits, wherein each of the plurality of load circuits includes a load current source, and wherein each of the plurality of current source circuits (shares a bias line in common with one of the load current sources.

With respect to claim 28, in addition to other elements in the claim prior art considered individual or combination does not teach or suggest: a circuit for reducing the current density, comprising: a third current source circuit that is arranged to provide a third local current at the first output of the third amplifier circuit such that at least a portion of the first half of the third differential current is prevented from being carried on the third bus; and a fourth current source circuit that is arranged to provide a fourth local current at the second output of the fourth amplifier circuit such that at least a portion of the second half of the third differential current is prevented from being carried on the fourth bus.

Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Rexford Barnie can be reached at (571) 272-7492. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

LINH NGUYEN
PRIMARY EXAMINER

12/10/06

Linh Van Nguyen

Art Unit 2819